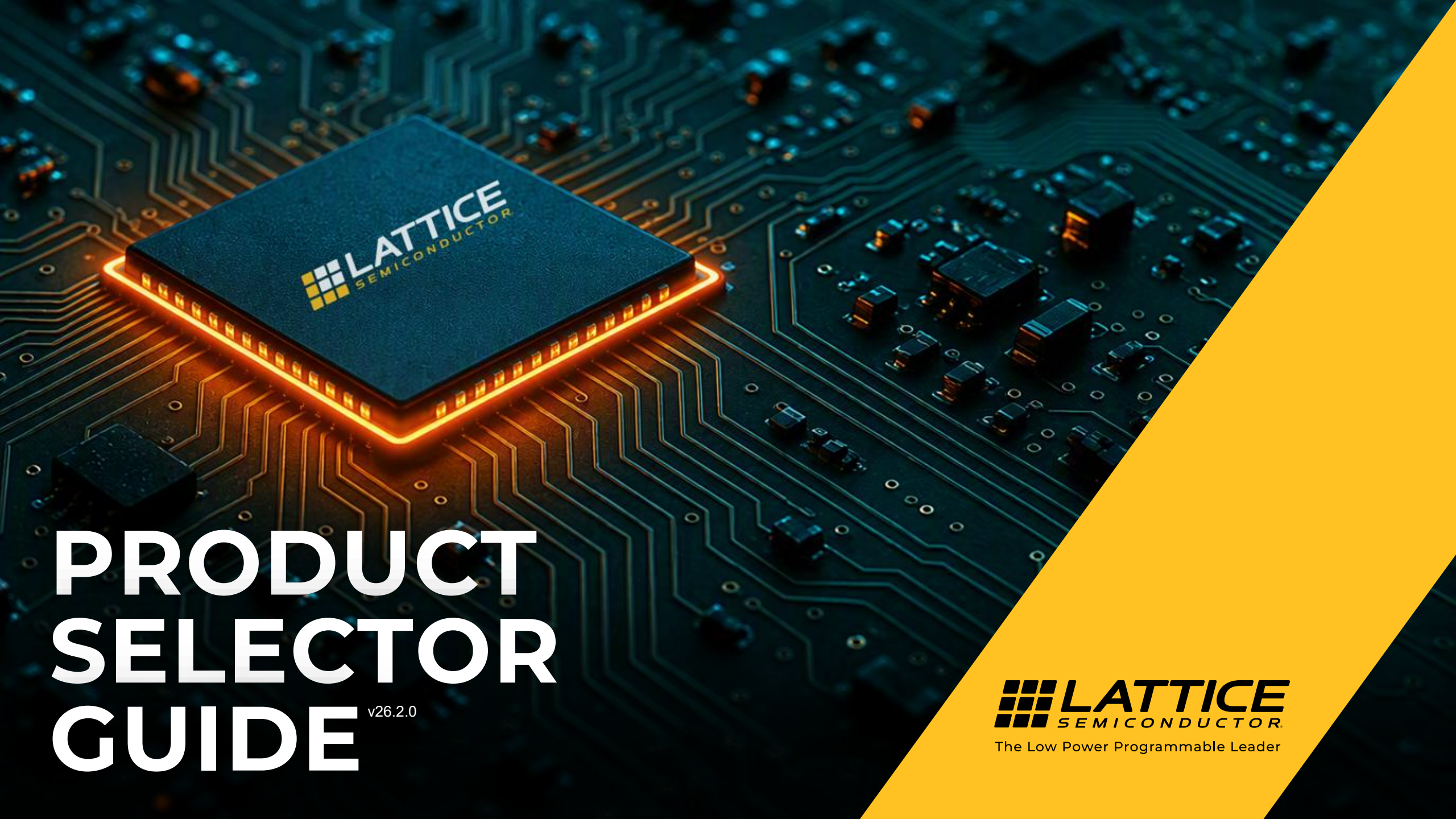


PRODUCT SELECTOR GUIDE

v26.2.0

LATTICE SEMICONDUCTOR

The Low Power Programmable Leader

Lattice FPGA Family

Market	Platform	Family	Typical Application
Small FPGA	**Foundation**	MachXO3 MachXO3D	Secure, low-power, instant-on FPGA for control and bridging
		MachXO4 MachXO4 RoT	
	Nexus	Certus-NX CertusPro-NX	General purpose, low-power FPGA with high I/O and reliability
		CrossLink-NX	Video connectivity with MIPI D-PHY and USB
		MachXO5-NX MachXO5TDQ-NX	Secure, high-density FPGA advanced control system
	Nexus 2	Certus-N2	General purpose, balance low-power/high-performance with secure and high-speed interfaces
		Mach-N2	Control and secure focused FPGA with high-speed interfaces
Mid FPGA	**Avant**	Avant-E	Low-power, high-performance FPGA for edge AI processing
		Avant-G	Low-power FPGA for general-purpose mid-range applications
		Avant-X	High-speed FPGA for secure, bandwidth-intensive systems

MachXO3 / MachXO3D Family

Features		MachXO3L/LF						MachXO3D	
		LCMXO3L/LF-640	LCMXO3L/LF-1300	LCMXO3L/LF-2100	LCMXO3L/LF-4300	LCMXO3L/LF-6900	LCMXO3L/LF-9400	LCMXO3D-4300	LCMXO3D-9400
Logic	LUT4 (LUT)	640	1300	2100	4300	6900 [1]	9400 [1]	4300	9400
Memory	EBR SRAM (kbits)	64	64	74	92	240	432	92	432
	Distributed RAM (kbits)	5	10	16	34	54	73	34	73
Configuration	User Flash Memory (kbits) (MachXO3LF Only)	64	64	80	96	256	448	367/1122 [2]	1088/2693 [2]
	Configuration Memory	On-chip Non-Volatile Configuration Memory (MachXO3L) On-chip Flash Memory (MachXO3LF)						On-chip Flash Memory	
	Dual Boot	External						On-Chip / External	
Embedded Function Block	I2C	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1
	Timer	1	1	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1	1	1
	Security	--	--	--	--	--	--	1	1
Other Features	MIPI D-PHY Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes [3]	Yes [3]
	I3C Compatible I/O	--	--	--	--	--	--	Yes [4]	Yes [4]
Device Options (Core Voltage)	Device E (1.2 V)	Yes	Yes	Yes	Yes	Yes	Yes	--	--
	Device C (2.5 - 3.3 V)	--	Yes	Yes	Yes	Yes	Yes	--	--
	Device HE (1.2 V)	--	--	--	--	--	--	--	Yes
	Device ZC/HC (2.5 - 3.3 V)	--	--	--	--	--	--	Yes	Yes
Temperature Grade	Commercial/Industrial/Automotive	C, I, A	C, I, A	C, I, A	C, I, A	C, I	C, I	C, I, A	C, I, A

Package (Type, Dimensions, Pitch)	Total I/O (Device Option)						Total I/O (Device Option)	
UWG36 (WLCSP, 2.5 x 2.5 mm, 0.4 mm)		28[5] (E)						
UWG49 (WLCSP, 3.2 x 3.2 mm, 0.4 mm)			38[5] (E)					
UWG81 (WLCSP, 3.8 x 3.8 mm, 0.4 mm)				63[5] (E)				
MG121 (csfBGA, 6 x 6 mm, 0.5 mm)	100[5] (E)	100[5] (E)	100[5] (E)	100[5] (E)				
MG132 (csBGA, 8 x 8 mm, 0.5 mm)	104 (E)	104 (E/C)	104 (E/C)	104 (E/C)				
MG256 (csfBGA, 9 x 9 mm, 0.5 mm)		206[5] (E)	206[5] (E)	206[5] (E)	206[5] (E)	206[5] (E)		
MG324 (csfBGA, 10 x 10 mm, 0.5 mm)			268[5] (E)	268[5] (E)	268[5] (E)			
SG72 (QFN, 10 × 10 mm, 0.5 mm)							58 (HC/ZC)	58 (HC/ZC)
TG100 (TQFP, 14 x 14 mm, 0.5 mm)	79 (E)	79 (E/C)	79 (E/C)					
UTG69 (WLCSP, 6.2 × 5.2 mm, 0.65 mm)								58 (HE)
BG256 (caBGA, 14 x 14 mm, 0.8 mm)		206[5] (C)	206[5] (C)	206[5] (C)	206[5] (C)	206[5] (C)	206 (HC[6]/ZC)	206 (HC/ZC/HE[6])
BG324 (caBGA, 15 x 15 mm, 0.8 mm)			279 (E/C)	279 (E/C)	279 (C)			
BG400 (caBGA, 17 x 17 mm, 0.8 mm)				335[5] (C)	335[5] (C)	335[5] (C)		335 (HC/ZC)
BG484 (caBGA, 19 x 19 mm, 0.8 mm)						384 (E/C)		383 (HC/ZC[6]/HE[6])
FTG256 (ftBGA, 17 × 17 mm, 1.0 mm)							206 (HC)	

Notes
1. Refer to Power and Thermal Estimation and Management for MachXO3 Devices (FPGA-TN-02059) for determination of safe ambient operating conditions.
2. When dual-boot is disabled, image space can be repurposed as extra UFM. Refer to MachXO3D UFM Size Table.
3. HC device only.
4. Four pairs of I/O in Bank 3 with I3C dynamic pull up capability.
5. Automotive device only for MachXO3LF. Only available in slowest speed grade.
6. Package is available for automotive devices only.

Temperature
C- Commercial
I- Industrial
A- Automotive

MachXO4 Family

Features		MachXO4 (Control)						MachXO4D (Secure Control)			
		LFMXO4-010	LFMXO4-015	LFMXO4-025	LFMXO4-050	LFMXO4-080	LFMXO4-110	LFMXO4D-040	LFMXO4D-050	LFMXO4D-080	LFMXO4D-110
Logic	Logic Cells (kLC)	1.10	1.60	2.60	5.20	8.30	11.30	3.60	5.20	8.30	11.30
	LUT4 (LUT)	896	1280	2112	4320	6864	9400	3000	4320	6864	9400
Memory	EBR SRAM (kbits)	64	64	74	92	240	432	80	92	240	432
	Distributed RAM (kbits)	10	10	16	34	54	73	34	34	73	73
Configuration	User Flash Memory (kbits)	64	64	80	96	256	448	367 / 1122[1]	367 / 1122[1]	1088 / 2693[1]	1088 / 2693[1]
	Configuration Memory	On-chip Flash Memory						On-chip Flash Memory			
	Dual Boot	External						On-Chip / External			
Embedded Function Block	I2C	2	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1	1
	Timer	1	1	1	1	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1	1	1	1	1
	Security	--	--	--	--	--	--	1	1	1	1
Other Features	MIPI D-PHY Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes[2]	Yes[2]	Yes[2]	Yes[2]
	I3C Compatible I/O	--	--	--	--	--	--	Yes[3]	Yes[3]	Yes[3]	Yes[3]
Device Options (Core Voltage)	Device ZC (2.5 - 3.3 V)	--	--	--	--	--	--	Yes	Yes	Yes	Yes
	Device HC (2.5 - 3.3 V)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Device HE (1.2 V)	Yes	Yes	Yes	Yes	Yes	Yes	--	--	Yes	Yes
Temperature Grade	Commercial/Industrial/Automotive	C, I, A	C, I, A	C, I, A	C, I, A	C, I	C, I	C, I, A[4]	C, I, A[4]	C, I, A[4]	C, I, A[4]

Package (Type, Dimensions, Pitch)	Total I/O (Device Option)						Total I/O (Device Option)			
UUG36[9] (WLCSP, 2.5 x 2.5 mm, 0.4 mm)		27 (HE)								
UUG49[9] (WLCSP, 3.2 x 3.2 mm, 0.4 mm)			37 (HE)							
UUG81[9] (WLCSP, 3.8 x 3.8 mm, 0.4 mm)				62 (HE)						
BSG132 (csBGA, 8 x 8 mm, 0.5 mm)	102 [1] (HC/HE)	102 [1] (HC/HE)	102 [1] (HC/HE)	102 [1] (HC/HE)			102 (ZC/HC)	102 (ZC/HC)		
TSG100 (TQFP, 14 x 14 mm, 0.5 mm)	78 [1] (HC/HE)	78 [1] (HC/HE)	78 [1] (HC/HE)							
TSG144 (TQFP, 20 x 20 mm, 0.5 mm)	105 (HC/HE)	105 (HC/HE)	109 (HC/HE)	112 (HC/HE)			112 (ZC/HC)	112 (ZC/HC)		
UTG69 (WLCSP, 5.2 x 6.2 mm, 0.65 mm)									57 (HE)	57 (HE)
BTG256 (caBGA, 12 x 12 mm, 0.65 mm)							204 (ZC/HC)	204 (ZC/HC)	204 (ZC/HC/HE)	204 (ZC/HC/HE)
BTG400 (caBGA, 12 x 12 mm, 0.65 mm)									333 (ZC/HC/HE)	333 (ZC/HC/HE)
BBG256 (caBGA, 14 x 14 mm, 0.8 mm)		204 [1] (HC/HE)	204 [1] (HC/HE)	204 [1] (HC/HE)	204 [1] (HC/HE)	204 [1] (HC/HE)	204 [4] (ZC/HC)	204 [4] (ZC/HC)	204 [4] (ZC/HC/HE)	204 [4] (ZC/HC/HE)
BBG400 (caBGA, 17 x 17 mm, 0.8 mm)				333 (HC/HE)	333 (HC/HE)	333 (HC/HE)			333 (ZC/HC/HE)	333 (ZC/HC/HE)
BBG484 (caBGA, 19 x 19 mm, 0.8 mm)						382 (HC/HE)				381 [4] (ZC/HC/HE)
BFG256 (ftBGA, 17 × 17 mm, 1.0 mm)		204 (HC/HE)	204 (HC/HE)	204 (HC/HE)			204 (ZC/HC)	204 (ZC/HC)		

Notes
1. When dual-boot is disabled, image space can be repurposed as extra UFM. Refer to MachXO4 RoT UFM Size Table.
2. HC device only.
3. Four pairs of I/O in Bank 3 with I3C dynamic pull up capability.
4. Package is available for automotive devices. Only available in slowest speed grade.

Temperature
C- Commercial
I- Industrial
A- Automotive

Certus-NX / CertusPro-NX Family

Features		Certus-NX (Logic Optimized)				Certus-NX (I/O Optimized)				CertusPro-NX	
		LFD2NX-9	LFD2NX-17	LFD2NX-28	LFD2NX-40	LFD2NX-15	LFD2NX-25	LFD2NX-35	LFD2NX-65	LFCPNX-50	LFCPNX-100
Logic	Logic Cells (kLC)[1]	9	17	28	39	15	25	35	65	52	96
	LUT4 (LUT)	7500	14166	23333	32500	12500	20833	29166	54166	43333	80000
Memory	EBR SRAM (kbits)	270	432	1044	1512	864	1440	1890	2304	1728	3744
	EBR LRAM (kbits)	1536	2560	1024	1024	512	512	512	1024	2048	3584
	Distributed RAM (kbits)	57	108	180	252	108	180	232	432	344	639
DSP Blocks	18 x 18 Multipliers	12	24	40	56	12	20	48	128	96	156
High Speed Connectivity	PCIe Hard IP	--	--	Gen 2.0	Gen 2.0	--	--	Gen 2.0	Gen 2.0	Gen 3.0	Gen 3.0
	PCIe / SERDES Max Speed (Gbps)[2]	--	--	5	5	--	--	5	5	10.1325	10.1325
Other Features	DDR Memory Support	--	--	DDR3/DDR3L (Up to 1066 Mbps)				--	--	LPDDR2 (Up to 800 Mbps), DDR3/DDR3L, LPDDR4 (Up to 1066 Mbps)	
	ADC Channels[3]	2	2	2	2	2	2	2	2	2	2
	Security	AES256 Bitstream Encryption, ECDSA Bitstream Authentication, SHA & HMAC Hashing, TRNG, AES128/256 Encryption									

Package (Type, Dimensions, Pitch)	Total I/O (Wide Range, High Performance, ADC) / SERDES Lane Temperature Grade									
MG121 (csfBGA, 6 x 6 mm, 0.5 mm)	77 (23,48,6) / 0 C, I, A	77 (23,48,6) / 0 C, I, A	81 (23,58,0) / 1 C, I, A	81 (23,58,0) / 1 C, I, A						
ASG256 (FOWLCSP, 9 x 9 mm, 0.5 mm)									165 (75,84,6) / 4 C, I, A	165 (75,84,6) / 4 C, I, A
BG196 (caBGA, 12 x 12 mm, 0.8 mm)	77 (23,48,6) / 0 C, I, A	77 (23,48,6) / 0 C, I, A	156 (92,58,6) / 0 C, I, A	156 (92,58,6) / 0 C, I, A						
BG256/CBG256 (caBGA, 14 x 14 mm, 0.8 mm)			191 (111,74,6) / 1 C, I, A	191 (111,74,6) / 1 C, I, A	205 (159,40,6) / 0 C, I	205 (159,40,6) / 0 C, I	181 (145, 30, 6) / 1 C, I	181 (145, 30, 6) / 1 C, I	165 (75,84,6) / 4 C, I, A	165 (75,84,6) / 4 C, I, A
BG400 (caBGA, 17 x 17 mm, 0.8 mm)					311 (257,48,6) / 0 C, I	311 (257,48,6) / 0 C, I	313 (259,48,6) / 0 C, I	313 (259,48,6) / 0 C, I		
BG484/BBG484[4] (caBGA, 19 x 19 mm, 0.8 mm)							371 (317,48,6) / 1 C, I	371 (317,48,6) / 1 C, I	269 (167,96,6) / 4 C, I, A	305 (167,132,6) / 8 C, I, A
BFG484[5] (BGA(Wirebond), 23 x 23 mm, 1.0 mm)									269 (167,96,6) / 4 C, I	305 (167,132,6) / 4 C, I
LFG672 (Lidless fcBGA, 27 x 27 mm, 1.0 mm)										305 (167,132,6) / 8 C, I

Notes
1. Logic Cells = LUT4 × 1.2 effectiveness.
2. Each SERDES lane consists of a Tx and Rx complement pair. See datasheet for protocols supported.
3. ADC available in –8 and –9 speed grades. Each ADC has a dedicated differential pair of input pins and a VREF pin.
4. BBG package can support SerDes standards with data rate up to 6.25 Gbps.
5. BFG package can support SerDes standards with data rate up to 5.5 Gbps.

Temperature
C- Commercial
I- Industrial
A- Automotive

CrossLink-NX Family

Features		CrossLink-NX			CrossLinkU-NX
		LIFCL-17	LIFCL-33	LIFCL-40	LIFCL-33U
Logic	Logic Cells (kLC) [1]	17	33	39	33
	LUT4 (LUT)	14166	27500	32500	27500
Memory	EBR SRAM (kbits)	432	1152	1512	1152
	EBR LRAM (kbits)	2560	2560	1024	2560
	Distributed RAM (kbits)	108	220	252	220
DSP Blocks	18 x 18 Multipliers	24	64	56	64
High Speed Connectivity	PCIe Hard IP	--	--	Gen 2.0	--
	SERDES Max Speed (Gbps)	--	--	5	--
MIPI	Hardened 10 Gbps D-PHY Quads [2]	2	--	2	--
	Hardened 2.5 Gbps D-PHY Data Lanes (Total) [2]	8	--	8	--
USB	USB 2.0 / USB 3.2 Gen 1 Interface	--	--	--	1 / 1
Other Features	DDR Memory Support	DDR3/DDR3L, LPDDR2 (Up to 1066 Mbps)	--	DDR3/DDR3L, LPDDR2 (Up to 1066 Mbps)	--
	ADC Channels [3]	1	--	1	--
	Security	AES256 Bitstream Encryption, ECDSA Bitstream Authentication, SHA & HMAC Hashing, TRNG, AES128/256 Encryption			

Package (Type, Dimensions, Pitch)	Total I/O (Wide Range, High Performance, ADC) / (D-PHY Quads[4], SERDES Lane[5]) Temperature Grade			
UWG72 (WLCSP, 3.8 × 4.1 mm, 0.4 mm)	39 (15, 24, 0) / (1, 0) C, I			
USG84 (WLCSP, 3.1 × 7.3 mm, 0.5 mm)		60 (34, 26) / (0, 0) C, I		44 (17, 27) / (0, 0) C, I
MG121 (csfBGA, 6 × 6 mm, 0.5 mm)	71 (23, 48, 0) / (2, 0) C, I, A		71 (23, 48, 0) / (2, 0) C, I, A	
MG289 (csBGA, 9.5 × 9.5 mm, 0.5 mm)			179 (99, 74, 6) / (2, 1) C, I	
SG72 (QFN, 10 × 10 mm, 0.5 mm)	40 (18, 22, 0) / (1, 0) C, I		39 (17, 22, 0) / (1, 0) C, I	
CTG104 (FCCSP, 5.5 x 8.5 mm, 0.65 mm)				52 (20, 32) / (0, 0) C, I
BG256 (caBGA, 14 × 14 mm, 0.8 mm)	77 (23, 48, 6) / (2, 0) C, I, A		162 (82, 74, 6) / (2, 1) C, I, A	
BG400 (caBGA, 17 × 17 mm, 0.8 mm)			191 (111, 74, 6) / (2, 1) C, I	

Notes
1. Logic Cells = LUT4 × 1.2 effectiveness.
2. Additional soft D-PHY Tx/Rx interfaces (at up to 1.5 Gbps per lane) are available using sysI/O.
3. ADC available in –8 and –9 speed grades. Each ADC has a dedicated differential pair of input pins and a VREF pin
4. Each D-PHY quad consists of 4 D-PHY data lanes.
5. Each SERDES lane consists of a Tx and Rx complement pair.

Temperature
C- Commercial
I- Industrial
A- Automotive

MachXO5-NX Family

Features		MachXO5-NX (IO Optimized)						MachXO5-NX (Logic Optimized)			
		LFMXO5-15D[1]	LFMXO5-25	LFMXO5-20DQ/TDQ	LFMXO5-30DQ/TDQ	LFMXO5-35/T	LFMXO5-65/T	LFMXO5-55T	LFMXO5-55TD[1]	LFMXO5-55TDQ	LFMXO5-100T
Logic	**Logic Cells (kLC) [2]**	14	27	20	30	35	65	53	53	38	96
	LUT4 (LUT)	11666	22500	16666	25000	29166	54166	44166	44166	31666	80000
Memory	**EBR SRAM (kbits)**	360	1440	756	828	1890	2304	2988	2988	1206	3744
	EBR LRAM (kbits)	512	512	512	512	512	1024	2,560	2560	3072	3,584
	Distributed RAM (kbits)	112	184	122	190	260	300	320	320	248	639
DSP Blocks	**18 x 18 Multipliers**	16	20	48	48	48	128	146	110	93	156
High Speed Connectivity	**PCIe Hard IP**	--	--	Gen 2.0	Gen 2.0	Gen 2.0	Gen 2.0	Gen 2.0	Gen 2.0	Gen 2.0	Gen 2.0
	SERDES Max Speed (Gbps)	--	--	5	5	5	5	5	5	5	5
Flash Memory	**User Flash Memory (kbits)[3]**	8160	15360	16320	16320	21504	21504	79872	14880	14880	79872
Other Features	**DDR Memory Support**	DDR3, DDR3L (Up to 1066 Mbps)	DDR3, DDR3L (Up to 1066 Mbps)	--	--	--	--	DDR3, DDR3L, LPDDR4 (Up to 1066 Mbps)	DDR3, DDR3L, LPDDR4 (Up to 1066 Mbps)	DDR3, DDR3L, LPDDR4 (Up to 1066 Mbps)	DDR3, DDR3L, LPDDR4 (Up to 1066 Mbps)
	ADC Channels[4]	1	2	1	1	1	1	2	2	2	2
Security	**Bitstream Authentication**	ECDSA-384	ECDSA-256	ECDSA-384, XMSS/LMS[5]	ECDSA-384, XMSS/LMS[5]	ECDSA-256	ECDSA-256	ECDSA-256	ECDSA-384/521, RSA-3K/4K	ECDSA-384/521, XMSS/LMS, ML-DSA	ECDSA-256
	Highest Classic Crypto Services	AES-256, ECDSA-384, SHA/HMAC-384, TRNG	AES-256, ECDSA-256, SHA/HMAC-256, TRNG	AES-256, ECDSA-384, SHA/HMAC-512, TRNG	AES-256, ECDSA-384, SHA/HMAC-512, TRNG	AES-256, ECDSA-256, SHA/HMAC-256, TRNG	AES-256, ECDSA-256, SHA/HMAC-256, TRNG	AES-256, ECDSA-256, SHA/HMAC-256, TRNG	AES-256, ECDSA-521, SHA/HMAC-512, TRNG	AES-256, ECDSA-521, SHA/HMAC-512, TRNG	AES-256, ECDSA-256, SHA/HMAC-256, TRNG
	Highest PQC Crypto Services	--	--	XMSS/LMS[5]	XMSS/LMS[5]	--	--	--	--	XMSS/LMS, ML-DSA, ML-KEM	--

Package (Type, Dimensions, Pitch)	Total I/O (Wide Range, High Performance, ADC) / SERDES Lane Temperature Grade									
BBG256 (caBGA, 14 × 14 mm, 0.8 mm)	205 (159, 40, 6) / 0 C, I	205 (159, 40, 6) / 0 C, I	170 (134, 30, 6) / 1 C, I	170 (134, 30, 6) / 1 C, I	173 (137, 30, 6) / 1 C, I	173 (137, 30, 6) / 1 C, I				
BBG400 (caBGA, 17 × 17 mm, 0.8 mm)	305 (251, 48, 6) / 0 C, I	305 (251, 48, 6) / 0 C, I	315 (261, 48, 6) / 0 C, I	315 (261, 48, 6) / 0 C, I	318 (264, 48, 6) / 0 C, I	318 (264, 48, 6) / 0 C, I	297 (159, 132, 6) / 2 C, I	297 (159, 132, 6) / 2 C, I	297 (159, 132, 6) / 2 C, I	297 (159, 132, 6) / 2 C, I
BBG484 (caBGA, 19x19mm, 0.8 mm)			368 (314, 48, 6) / 1 C, I	368 (314, 48, 6) / 1 C, I	371 (317, 48, 6) / 1 C, I	371 (317, 48, 6) / 1 C, I				

Notes
1. Enhanced security devices in the MachXO5-NX family support up to 521-bit strength security.
2. Logic Cells = LUT4 × 1.2 effectiveness.
3. Without memory initialization
4. ADC available in –8 and –9 speed grades. Each ADC has a dedicated differential pair of input pins and a VREF pin.
5. PQC services available only in TDQ devices

Temperature
C- Commercial
I- Industrial

Certus-N2 Family

Features		Certus-N2			
		LN2-CT06	LN2-CT10	LN2-CT16	LN2-CT20
Logic	System Logic Cells (kSLC)	65	100	160	220
	LUT4 (LUT)	40000	61000	98000	135000
Memory	EBR SRAM (Mbits)	4	5.5	8	11.4
	Distributed RAM (kbits)	416	636	1041	1272
DSP Blocks	18 x 18 Multipliers	120	240	360	520
High Speed Connectivity	PCIe Hard IP	Gen 4.0	Gen 4.0	Gen 4.0	Gen 4.0
	SERDES Max Speed (Gbps)	16	16	16	16
Other Features	DDR Memory Support	LPDDR4, DDR4 (Up to 2400 Mbps)			
	Security	Bitstream Encryption & Authentication			

Package[1] (Type, Dimensions, Pitch)	Total I/O (Wide Range, High Performance) / SERDES Lane Temperature Grade			
ASGA273 (FOWLP, 9 × 9 mm, 0.5 mm)	112 (27, 85) / 4 C, I, A	112 (27, 85) / 4 C, I, A		
ASGA410 (FOWLP, 9 × 11 mm, 0.5 mm)			247[2] (94, 153) / 0 C, I, A	247[2] (94, 153) / 0 C, I, A
ASGA410 (FOWLP, 9 × 11 mm, 0.5 mm)			196 (43, 153) / 4 C, I, A	196 (43, 153) / 4 C, I, A
CBG256 (FCCSP, 14 × 14 mm, 0.8 mm)	153 (51, 102) / 2 C, I, A	153 (51, 102) / 2 C, I, A		
CBG484 (FCCSP, 18 × 18 mm, 0.8 mm)	196 (94, 102) / 4 C, I, A	196 (94, 102) / 4 C, I, A	247 (94, 153) / 4 C, I, A	247 (94, 153) / 4 C, I, A
LFG676 (fcBGA, 27 × 27 mm, 1.0 mm)			298 (43, 255) / 8 C, I, A	298 (43, 255) / 8 C, I, A

Notes
1. Refer to Ordering Information for more details.
2. Package option available in CT20E and CT16E only.

Temperature
C- Commercial
I- Industrial
A- Automotive

Mach-N2 Family

Features		Mach-N2				
		LN2-MH06	LN2-MH10	LN2-MH16	LN2-MH20	LN2-MH21D
Logic	System Logic Cells (kSLC)	65	100	160	220	215
	LUT4 (LUT)	40000	61000	98000	135000	132000
Memory	EBR SRAM (Mbits)	4	5.5	8	11.4	10.4
	Distributed RAM (kbits)	416	636	1041	1400	1370
DSP Blocks	18 x 18 Multipliers	120	240	360	520	520
High Speed Connectivity	PCIe Hard IP	Gen 4.0	Gen 4.0	Gen 4.0	Gen 4.0	Gen 4.0
	SERDES Max Speed (Gbps)	16	16	16	16	16
Flash Memory	User Flash Memory (kbits)	TBD	TBD	105472	105472	TBD
Other Features	DDR Memory Support	LPDDR4 DDR4 (Up to 2133 Mbps)				
Security	Bitstream Authentication	ECDSA-521 RSA4096				
	Post Quantum Cryptography	--	--	--	--	Supported

Package[1] (Type, Dimensions, Pitch)	Total I/O (Wide Range, High Performance) / SERDES Lane Temperature Grade				
CBG256 (FCCSP, 14 × 14 mm, 0.8 mm)	141 (39, 102) / 2 C, I	141 (39, 102) / 2 C, I			
CBG484 (FCCSP, 18 × 18 mm, 0.8 mm)	196 (94, 102) / 4 C, I	196 (94, 102) / 4 C, I	248 (94, 156) / 4 C, I	248 (94, 156) / 4 C, I	236 (83, 153) / 4 C, I

Notes
1. Refer to Ordering Information for more details.

Temperature
C- Commercial
I- Industrial
A- Automotive

Avant-E/G/X Family

Features		Avant-E			Avant-G			Avant-X		
		LAV-AT-E30	LAV-AT-E50	LAV-AT-E70	LAV-AT-G30	LAV-AT-G50	LAV-AT-G70	LAV-AT-X30	LAV-AT-X50	LAV-AT-X70
Logic	System Logic Cells (kLC)	262	409	637	262	409	637	262	409	637
	LUT4 (LUT)	163000	255000	397000	163000	255000	397000	163000	255000	397000
Memory	EBR SRAM (Mbits)	14.4	22.7	35.6	14.4	22.7	35.6	14.4	22.7	35.6
	Distributed RAM (Mbits)	1.7	2.66	4.14	1.7	2.66	4.14	1.7	2.66	4.14
DSP Blocks	18 x 18 Multipliers	700	1120	1800	700	1120	1800	700	1120	1800
High Speed Connectivity	PCIe Hard IP	--	--	--	Gen 3.0	Gen 3.0	Gen 3.0	Gen 4.0	Gen 4.0	Gen 4.0
	SERDES Max Speed (Gbps)	--	--	--	12.5	12.5	12.5	25	25	25
Other Features	DDR Memory Support	LPDDR4/DDR4			LPDDR4/DDR4			LPDDR4/DDR4, DDR5 (Up to 2100 Mbps)		
	Security	Bitstream Encryption & Authentication			Bitstream Encryption & Authentication			Bitstream Encryption & Authentication, User Security		

Package [1] (Type, Dimensions, Pitch)	Total I/O (Wide Range, High Performance) Temperature Grade			Total I/O (Wide Range, High Performance) / SERDES Lane Temperature Grade					
ASGA410[2] (FOWLP, 9 × 11 mm, 0.5 mm)	247 (94, 153) C, I, A			196 (43, 153) / 4 C, I, A			196 (43, 153) / 4 C, I, A		
CSG841 (FCCSP, 15 × 15 mm, 0.5 mm)		553 (94, 459) C, I, A	553 (94, 459) C, I, A						
CBG484 (FCCSP, 18 × 18 mm, 0.8 mm)	349 (94, 255) C, I, A	349 (94, 255) C, I, A	349 (94, 255) C, I, A						
FBG644 (FCBGA, 19 x 23 mm, 0.8 mm)				298 (43, 255) / 12 C, I, A	298 (43, 255) / 12 C, I, A	298 (43, 255) / 12 C, I, A	298 (43, 255) / 12 C, I, A	298 (43, 255) / 12 C, I, A	298 (43, 255) / 12 C, I, A
LFG676[3] (FCBGA, 27 × 27 mm, 1.0 mm)			297 (42, 255) C, I, A	298 (43, 255) / 12 C, I, A	298 (43, 255) / 16 C, I, A	298 (43, 255) / 16 C, I, A	298 (43, 255) / 12 C, I, A	298 (43, 255) / 16 C, I, A	298 (43, 255) / 16 C, I, A
LFG1156[3] (FCBGA, 35 × 35 mm, 1.0 mm)			553 (94, 459) C, I, A			554 (95, 459) / 28 C, I, A			554 (95, 459) / 28 C, I, A

Notes
1. B variants only support limited package options. Refer to Ordering Information for more details.
2. SERDES performance is limited to 16G in this package.
3. Avant-E/G/X devices share the same WRIO and HPIO locations.

Temperature
C- Commercial
I- Industrial
A- Automotive

Foundation Portfolio Density Migratable Group

Package	MachXO3L/LF						MachXO3D	
	LCMXO3L/LF-640	LCMXO3L/LF-1300	LCMXO3L/LF-2100	LCMXO3L/LF-4300	LCMXO3L/LF-6900	LCMXO3L/LF-9400	LCMXO3D-4300	LCMXO3D-9400
MG121	◆	◆	◆	◆				
MG132	◆	◆	◆	◆				
MG256		◆	◆	◆	◆	◆		
MG324			◆	◆	◆			
SG72							◆	◆
TG100	◆	◆	◆					
BG256		◆	◆	◆	◆	◆	◆	◆
BG324			◆	◆	◆			
BG400				◆	◆	◆		◆
BG484						◆		◆

Package	MachXO4 (Control)						MachXO4 RoT (Secure Control)			
	LFMXO4-010	LFMXO4-015	LFMXO4-025	LFMXO4-050	LFMXO4-080	LFMXO4-110	LFMXO4D-040	LFMXO4D-050	LFMXO4D-080	LFMXO4D-110
BSG132	◆	◆	◆	◆			◆	◆		
TSG100	◆	◆	◆							
TSG144	◆	◆	◆	◆			◆	◆		
UUG69									◆	◆
BTG256							◆	◆	◆	◆
BTG400									◆	◆
BBG256		◆	◆	◆	◆	◆	◆	◆	◆	◆
BBG400				◆	◆	◆			◆	◆
BFG256		◆	◆	◆			◆	◆		

Nexus Portfolio Density Migratable Group

Package	Certus-NX (I/O Optimized)				Certus-NX (I/O Optimized)				CertusPro-NX	
	LFD2NX-9	LFD2NX-17	LFD2NX-28	LFD2NX-40	LFD2NX-15	LFD2NX-25	LFD2NX-35	LFD2NX-65	LFCPNX-50	LFCPNX-100
MG121	◆	◆	◆	◆						
ASG256									◆	◆
BG196	◆	◆	◆	◆						
BG256/CBG256			◆	◆	◆	◆	◆	◆	◆	◆
BG400					◆	◆	◆	◆		
BG484/BBG484							◆	◆	◆	◆
BFG484									◆	◆

Package	CrossLink-NX	
	LIFCL-17	LIFCL-40
MG121	◆	◆
SG72	◆	◆
BG256	◆	◆

Package	MachXO5-NX (I/O Optimized)						MachXO5-NX (Logic Optimized)			
	LFMXO5-15D	LFMXO5-25	LFMXO5-20TDQ	LFMXO5-30TDQ	LFMXO5-35/T	LFMXO5-65/T	LFMXO5-55T	LFMXO5-55TD	LFMXO5-55TDQ	LFMXO5-100T
BBG256			◆	◆	◆	◆				
BBG400	◆	◆	◆	◆	◆	◆	◆			◆
BBG484			◆	◆	◆	◆				

Nexus 2 Portfolio Density Migratable Group

Package	Certus-N2			
	LN2-CT06	LN2-CT10	LN2-CT16	LN2-CT20
ASGA273	◆	◆		
ASGA410			◆	◆
ASGA410			◆	◆
CBG256	◆	◆		
CBG484	◆	◆	◆	◆
LFG676			◆	◆

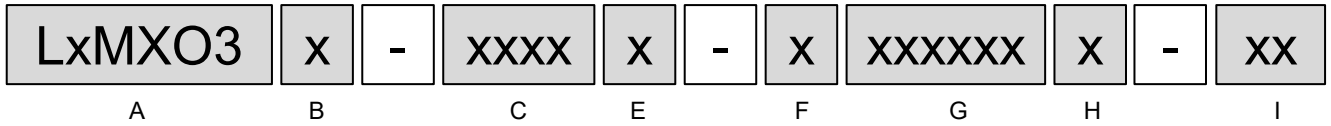
Package	Mach-N2				
	LN2-MH06	LN2-MH10	LN2-MH16	LN2-MH20	LN2-MH21D
CBG256	◆	◆			
CBG484	◆	◆	◆	◆	◆

Avant Portfolio Density Migratable Group

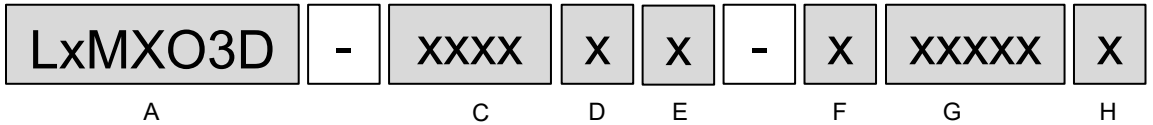
Package	Avant-E			Avant-G			Avant-X		
	LAV-AT-E30	LAV-AT-E50	LAV-AT-E70	LAV-AT-G30	LAV-AT-G50	LAV-AT-G70	LAV-AT-X30	LAV-AT-X50	LAV-AT-X70
CSG841		◆	◆						
CBG484	◆	◆	◆						
FBG644				◆	◆	◆	◆	◆	◆
LFG676				◆	◆	◆	◆	◆	◆

Part Number Description for Foundation FPGA

MachXO3 Family



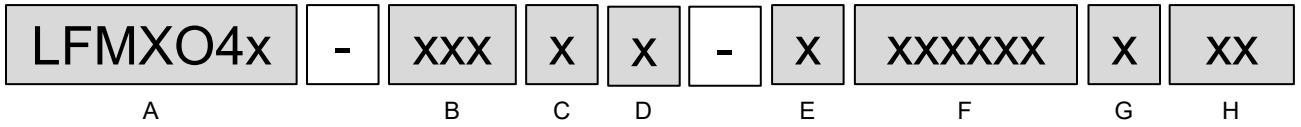
MachXO3D Family



	Attributes	MachXO3	MachXO3D
	Platform	Foundation	Foundation
A	**Device Family**	LCMXO3 = MachXO3 FPGA COM/IND LAMXO3 = MachXO3 FPGA AUTO	LCMXO3D = MachXO3D FPGA COM/IND LAMXO3D = MachXO3D FPGA AUTO
B	**Configuration Memory**	L= NVCM LF= Flash	--
C	**Logic Capacity Index**	640 – 9400	4300 – 9400
D	**Power/ Performance**	--	Z = Low Power H = High Performance
E	**Supply Voltage**	C = 2.5 V/3.3 V E = 1.2 V	C = 2.5 V/3.3 V E = 1.2 V
F	**Speed**	5 = Slowest 6 = Fastest	2 = Slowest (Low Power) 3 = Fastest (Low Power) 5 = Slowest (High Performance) 6 = Fastest (High Performance)
G	**Package**	UWG36 UWG49 UWG81 TG100 MG121 MG132 MG256 MG324 BG256 BG324 BG400 BG484	UTG69 SG72 BG256 BG400 BG484 FTG256
H	**Grade**	C = Commercial I = Industrial E = Automotive	C = Commercial I = Industrial E = Automotive
I	**Shipping Method**	Blank = Trays TR = Tape and Reel TR50 = WLCSP Package, 50 parts per reel TR1K = WLCSP Package, 1000 parts per reel	--

Part Number Description for Foundation FPGA

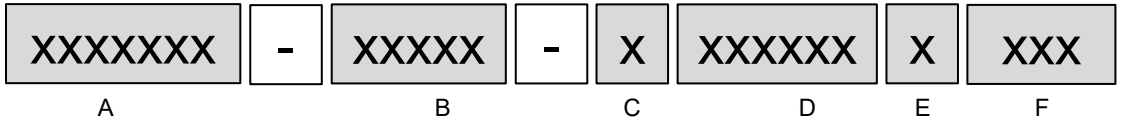
MachXO4 Family



	Attributes	MachXO4
	Platform	Foundation
A	**Device Family**	LFMXO4 = MachXO4 FPGA LFMXO4D = MachXO4 RoT FPGA
B	**Logic Capacity Index**	3000 – 9400
C	**Power/ Performance**	Z = Low Power H = High Performance
D	**Supply Voltage**	C = 2.5 V/3.3 V E = 1.2 V
F	**Speed**	2 = Slowest (Low Power) 3 = Fastest (Low Power) 5 = Slowest (High Performance) 6 = Fastest (High Performance)
G	**Package**	UUG36 UUG49 UUG81 BSG132 TSG100 TSG144 UTG69 BTG256 BTG400 BBG256 BBG400 BBG484 BFG256
H	**Grade**	C = Commercial I = Industrial A = Automotive
I	**Shipping Method**	Blank = Trays TR = Tape and Reel TR50 = 50 parts per reel TR1K = 1000 parts per reel

Part Number Description for Nexus FPGA

Certus-NX / Certus-Pro-NX / CrossLink-NX / MachXO5- NX Family



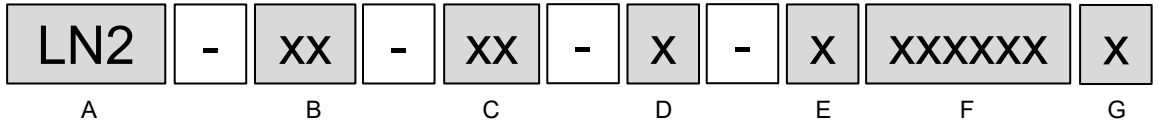
Attributes		Certus-NX / CertusPro-NX / CrossLink-NX / MachXO5-NX
	Platform	Nexus
A	**Device Family**	LFD2NX = Certus-NX FPGA LFCPNX = CertusPro-NX FPGA LIFCL = CrossLink-NX FPGA LFMXO5 = MachXO5-NX FPGA
B	**Logic Capacity Index**	9 – 100 Features: U = Hardened USB T = Transceiver D = Root of Trust DQ = Post Quantum Crypto Security and RoT
C	**Speed**[1]	7 = Slowest 8 = Mid-grade 9 = Fastest
D	**Package**	MG121 BG196 BG256 BG400 BG484 ASG256 CBG256 BBG484 BFG484 LFG672 UWG72 SG72 MG289 USG84 CTG104[2] BBG256 BBG400
E	**Grade**	C = Commercial I = Industrial A = Automotive
F	**Revision**[3]	01A

Notes

1. Same number for HP and LP:
   Certus-NX / CrossLink-NX: Input Comparator, ADC, EBR ECC, and DTR are only available in -7 (-A), -8 (-C/I), and -9 (-C/I) speeds and grades.
   CertusPro-NX: Input Comparator, ADC, EBR ECC, and DTR are only available in -7 (-A) and -8 (-A), -8 (-C/I), and -9 (-C/I) speeds and grades.
   MachXO5-NX: Input Comparator, ADC, EBR ECC, and DTR are only available in -8 (-C/I), and -9 (-C/I) speeds and grades.
2. ECC is only available on CTG104 -8 and -9 speed grade devices.
3. 01A die version does not support JTAG Boundary Scan feature.

Part Number Description for Nexus 2 FPGA

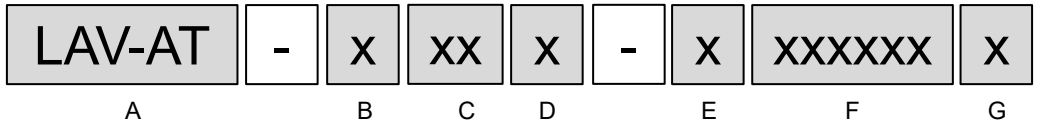
Certus-N2 / Mach-N2 Family



Attributes		Certus-N2	Mach-N2
A	**Platform Code**	LN2 = Lattice Nexus 2	LN2 = Lattice Nexus 2
B	**Device Family**	CT = Certus-N2	MH = Mach-N2
C	**Logic Capacity Index**	6 – 20	6 – 21
D	**Features**	E = Entry (No SERDES)	D = RoT and PQC
E	**Speed**	1 = Slowest 2 = Mid-grade 3 = Fastest	1 = Slowest 2 = Mid-grade 3 = Fastest
F	**Package**	ASGA273 ASG410 CBG256 CBG484 LFG676	CBG256 CBG484
G	**Grade**	C = Commercial I = Industrial A = Automotive	C = Commercial I = Industrial

Part Number Description for Avant FPGA

Avant-E / G / X Family



Attributes		Avant-E / G / X
A	**Platform Code**	LAV-AT = Lattice Avant
B	**Device Family**	E = Avant-E G = Avant-G X = Avant-X
C	**Logic Capacity Index**	30 – 70
D	**Silicon Variant**	(Blank) B = B Variant
E	**Speed**	1 = Slowest 2 = Mid-grade 3 = Fastest
F	**Package**	ASGA410 CSG841 CBG484 FBG644 LFG676 LFG1156
G	**Grade**	C = Commercial I = Industrial A = Automotive

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